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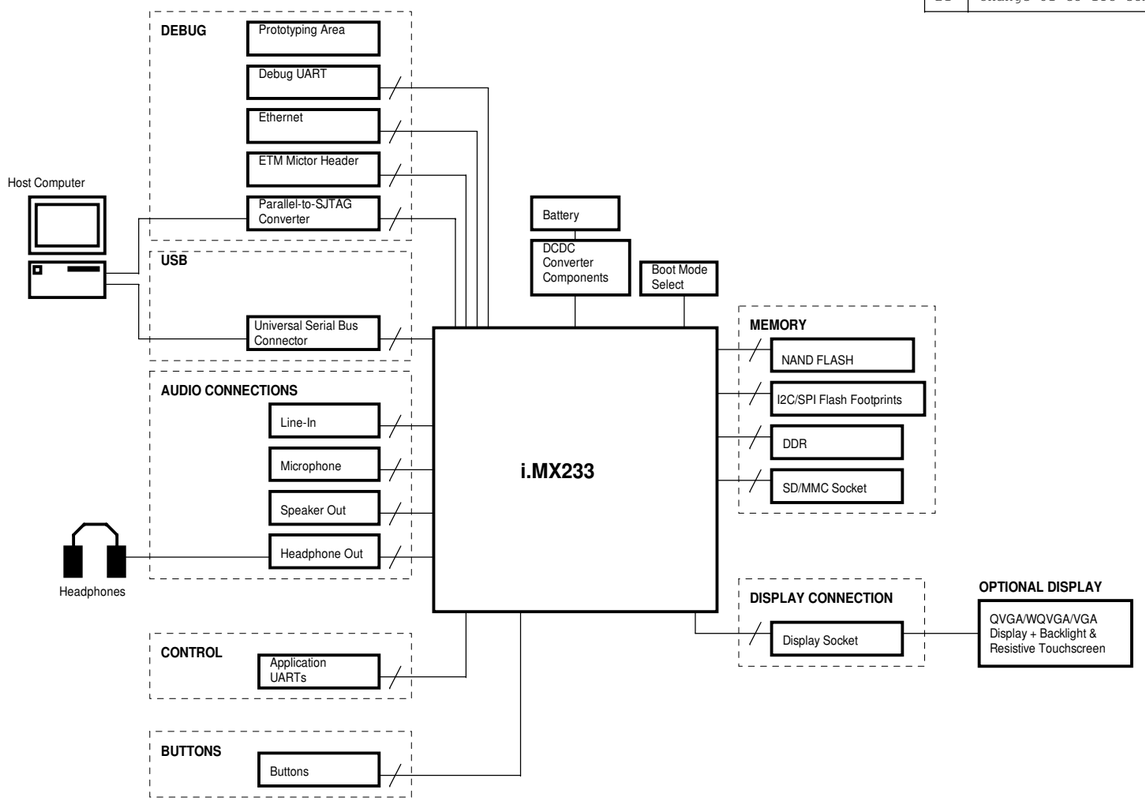
Revisions

Rev	Description	Date	Approved
X1	Original Release	06/04/09	Mark Midddleton
A	Release to Production	06/10/09	Mark Midddleton
A1	Change U1 Part number to i.MX233	06/29/09	Mark Midddleton
B	Changed U16 to REG104 Removed SSP1 traces to LCD. Changed default NAND. Changed R183 to 10K. Added Pull Up to Ethernet CS. Modified UART Enable circuit. Added isolation jumpers to SSP1 traces to expansion port. Added USB 5V to External 5V jumper opt. Modified OTG Host power circuitry. Changed U48 to MMA7455L and POP. Switched I2C_SDA/SCL on J38.	08/05/09	Mark Midddleton
B1	Change U1 to ITC compliant part.	08/21/09	Mark Midddleton

Block Diagram



freescale semiconductor

Multimedia Application Division, Wireless & Mobile System Group

ICAP Classification: FCP: FIUO: PXIBI:

Designer: Mark Middleton	Drawing Title: i.MX233 EVK		
Drawn by: DRAWN_BY	Page Title: TITLE PAGE		
Approved: <Approver>	Size: Custom	Document Number: SOURCE:SCH-77066 PDF:SPF-77066	Rev: B1
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GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

USAGE GUIDE

TO ENTER BATTERY-POWERED MODE

Set HOLD SWITCH (S1) = OFF

Set BOOT MODE SELECT DIPSWITCH (S36) = 0100 to selects boot from NAND.

Set USB5V SWITCH (S14) = OFF

Set DEBUG SWITCH (S22) = OFF

Set BATTERY SOURCE SWITCH (S22) according to power source. If an actual battery or external power supply is used, it should be connected at J21 or J13 and the BATTERY SOURCE SWITCH should be set to BATTERY. If the internal regulators are used, an AC Adapter should be connected to the J6 power jack and the BATTERY SOURCE SWITCH should be set to REGULATOR.

Then press POWER BUTTON (S2) to power on the player.

TO ENTER USB / 5V POWERED MODE

Set HOLD SWITCH (S1) = OFF

Set BOOT MODE SELECT DIPSWITCH (S36) = 0100 to selects boot from NAND.

Set DEBUG SWITCH (S22) = OFF

Set BATTERY SOURCE SWITCH (S22) according to power source. If an actual battery or external power supply is used, it should be connected at J21 or J13 and the BATTERY SOURCE SWITCH should be set to BATTERY. If no battery power supply is available or needed in USB mode the BATTERY SOURCE SWITCH should be set to BATTERY. If the internal regulators are used, an AC Adapter should be connected to J6 and the BATTERY SOURCE SWITCH should be set to REGULATOR.

USB5V SWITCH (S14) = ON

Connect a USB cable to the J4 USB jack and the device should power on and enumerate.

TO ENTER RECOVERY MODE

METHOD 1:

With USB disconnected, set the BOOT MODE SELECT DIPSWITCH (S36) to 0000 (Boot from USB). Connect USB cable (or flip USB5V switch to ON). Once the EVK enumerates in Device Manager as Player Recovery Device, set the BOOT MODE SELECT DIPSWITCH (S36) back to 0100.

METHOD 2:

Ensure DEBUG SWITCH (S22) is set to OFF. With USB disconnected, press and hold the RECOVERY BUTTON (S25), and then connect USB cable (or flip USB5V switch to ON). Continue to hold the RECOVERY BUTTON for 5 seconds or until the Player Recovery Device appears in the Device Manager.

TO ENTER DEBUG MODE

Set HOLD SWITCH (S1) = OFF

Set BOOT MODE SELECT DIPSWITCH (S36) = 0100 to selects boot from NAND.

Set USB5V SWITCH (S14) depending on which mode you wish to debug.

Connect the Slingshot JTAG cable to the J2 JTAG Port.

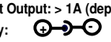
Set BATTERY SOURCE SWITCH (S22) according to power source. If an actual battery or external power supply is used, it should be connected at J21 or J13 and the BATTERY SOURCE SWITCH should be set to BATTERY. If the internal regulators are used, an AC Adapter should be connected to J6 and the BATTERY SOURCE SWITCH should be set to REGULATOR.

Set DEBUG SWITCH (S22) = ON

AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC

Current Output: > 1A (depending on application)

Polarity: 

Inner Diameter: 2.1mm

Outer Diameter: 5.5mm

SWITCH OPERATION

BATTERY SOURCE SWITCH (S12)

BATTERY:

Allows the board to be powered from either the J21 header or the J13 connector. Note that J21 and J13 are wire in parallel, so power should only be applied to one of the two inputs at any time. Allowable input voltage ranges:
3.0V to 4.2V (nominal 3.7V)

REGULATOR:

Uses the onboard regulator as the power source for the DC-DC converters. The regulators are adjustable through external resistors or a potentiometer, but the default value is 4.20V

USB5V SWITCH (S14)

ON:

Connects USB5V to the VDD5V pin on the i.MX233. If a USB cable is attached, this should allow the device to power up and enumerate.

OFF:

Disconnects USB5V from the EVK. Can be used to force a USB disconnect and re-enumeration without unplugging the USB cable.

DEBUG SWITCH (S22)

ON:

Allows use of the Serial JTAG port for development or debug.

OFF:

Normal (non-debug) operation.

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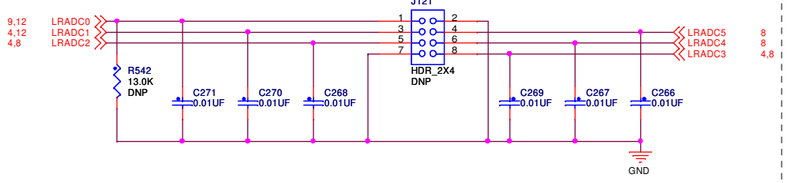
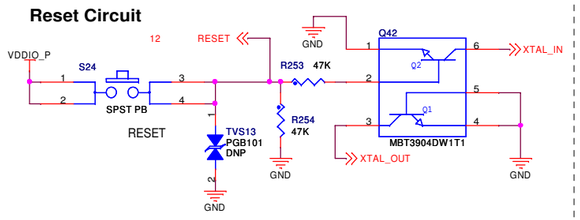
i.MX233 169-Pin BGA

Resistive Touchscreens Capacitors



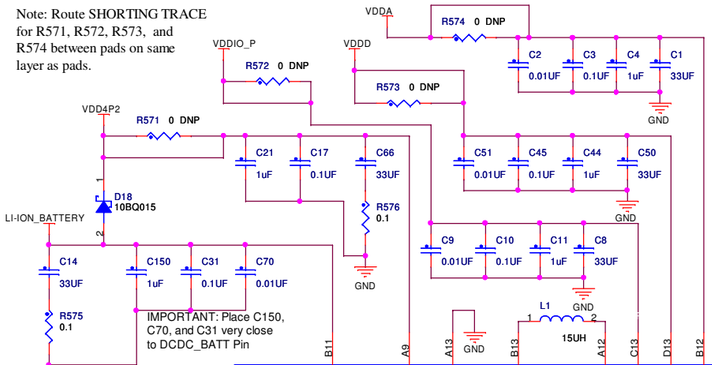
Reset Circuit

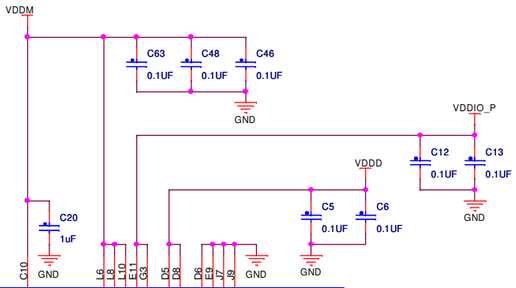


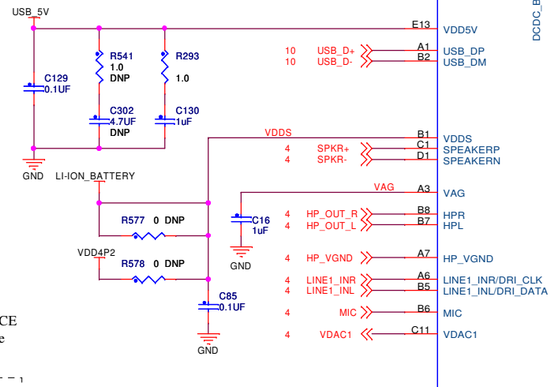
The i.MX233 should use low-ESR (~300mOhms) tantalums or ceramics for both the VDD4P2 and the LI-ION BATTERY supplies to prevent a battery charger oscillation issue.

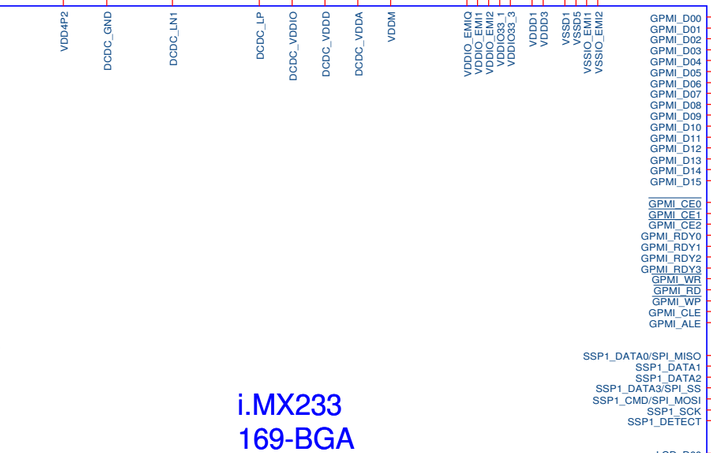
Note: Route SHORTING TRACE for R571, R572, R573, and R574 between pads on same layer as pads.

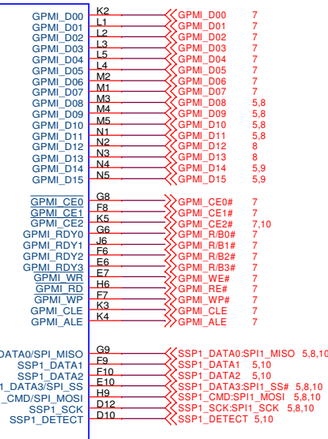
C1, C8, C50 should be a low-ESR tantalum or ceramic (<400mOhms) to reduce power supply noise. Ceramic capacitors are recommended. Do not use Y5R.

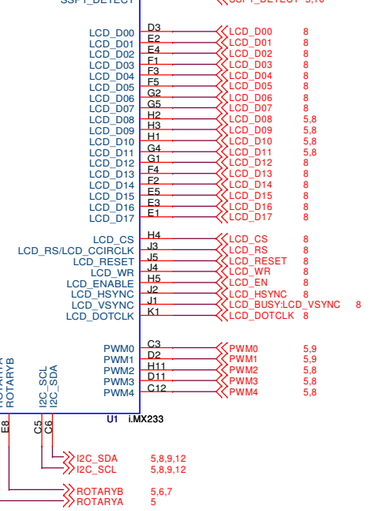


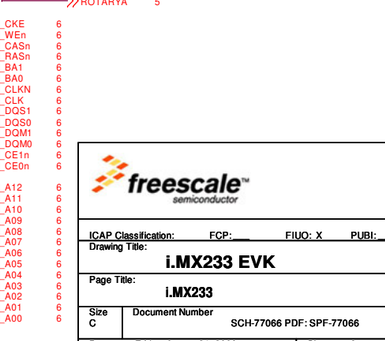


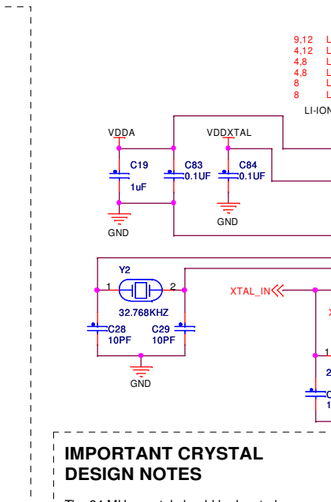


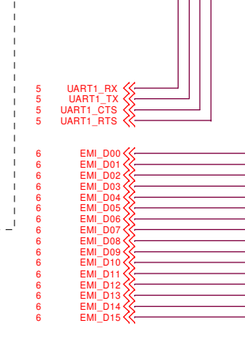


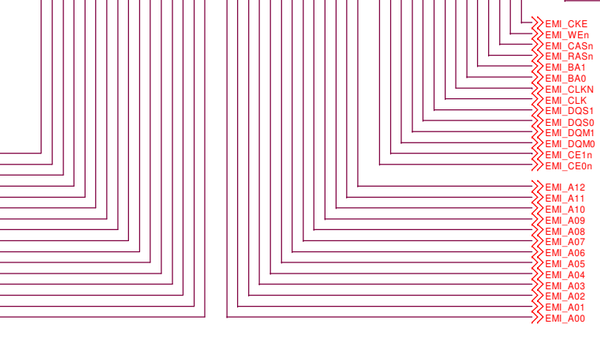










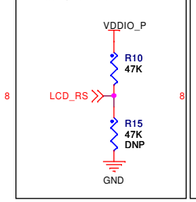


i.MX233
169-BGA

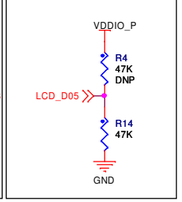
i.MX233 BOOT MODE SELECT

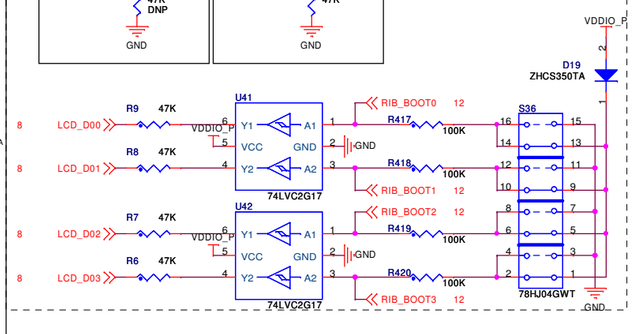
BOOT MODE	LCD DATA 03	02	01	00
USB	0	0	0	0
3.3V I2C Master	0	0	0	1
3.3V SPI Flash 1 Master	0	0	1	0
3.3V SPI Flash 2 Master	0	0	1	1
3.3V NAND	0	1	0	0
DEBUG	0	1	1	0
3.3V SD/MMC 1	1	0	0	1
3.3V SD/MMC 2	1	0	1	0

LCD_RS needs to be pulled HIGH to enable Resistor Boot Mode. If LCD_RS is pulled low, the i.MX233 will attempt to boot from OTP.



LCD_D05 = ETM Enable Bit:
Low = ETM disabled
High = ETM enabled





IMPORTANT CRYSTAL DESIGN NOTES

The 24 MHz crystal should be located close to the i.MX233. Consult crystal manufacturer datasheet for recommended load capacitor values (typically 10-18pF).

Cload = [(C26*C27) / (C26+C27)] + Cstray

where Cstray = stray PCB capacitance, typically 4 - 6 pF

Note: For Microsoft DRM applications use a 30 ppm crystal.

POWER TESTPOINTS

GROUND TESTPOINTS

NOTE: The VAG capacitor ground must route to star ground at VSSA2.

Note: Route SHORTING TRACE for R577 between pads on same layer as pads.

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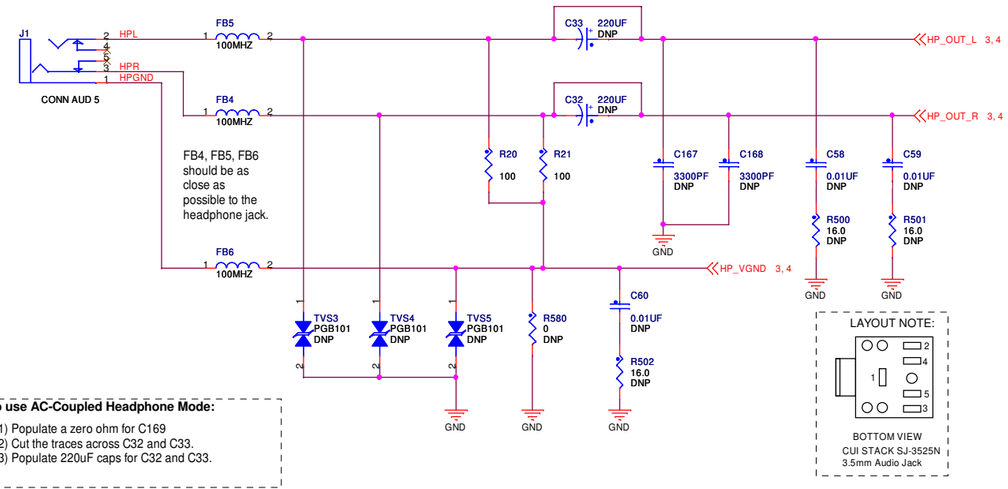
Headphone

Note: Route SHORTING TRACE for C32 and C33 between pads on same layer as pads.



FB4, FB5, FB6 should be as close as possible to the headphone jack.

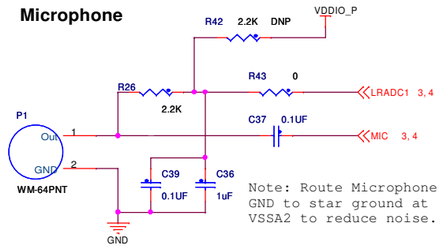
LAYOUT NOTE:

BOTTOM VIEW
CUI STACK SJ-3525N
3.5mm Audio Jack

To use AC-Coupled Headphone Mode:

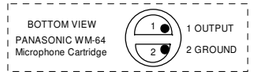
1) Populate a zero ohm for C169
2) Cut the traces across C32 and C33.
3) Populate 220uF caps for C32 and C33.

Microphone

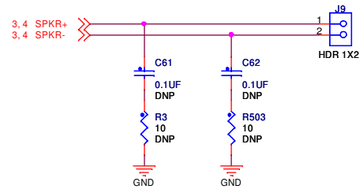


Note: Route Microphone GND to star ground at VSSA2 to reduce noise.

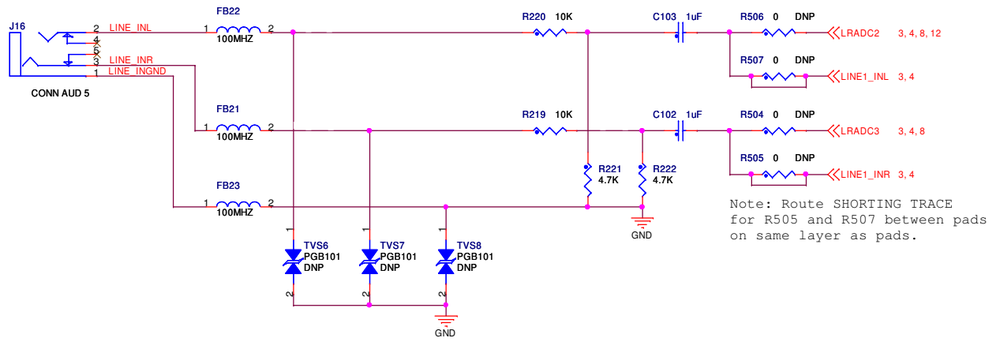
The microphone is configured for LRADC1 bias by default. If LRADC1 is not available, VDDIO bias can be used by cutting the trace between R43 pads and populating R42.



External Speaker

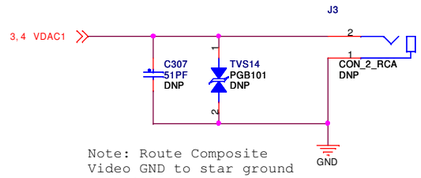


Line-In Circuit



Note: Route SHORTING TRACE for R505 and R507 between pads on same layer as pads.

Optional Composite Video



Note: Route Composite Video GND to star ground at VSSA2.

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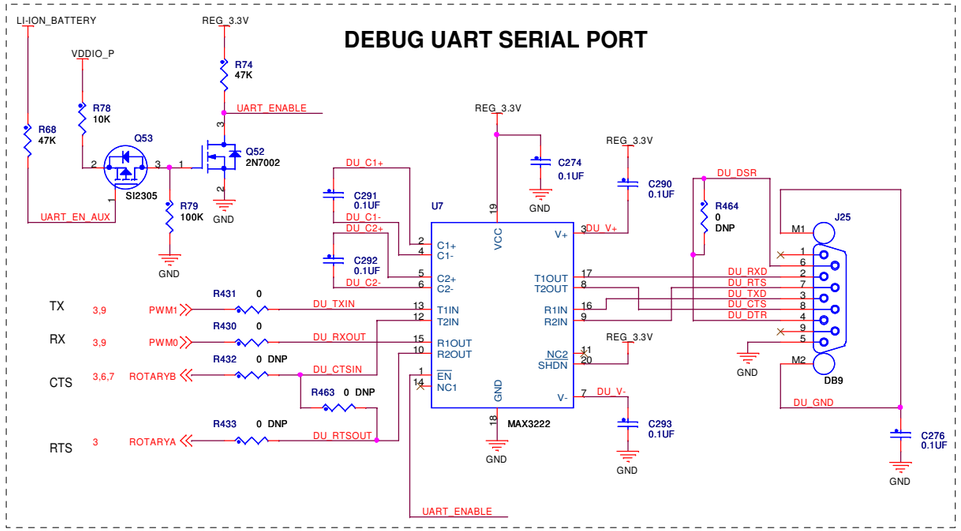
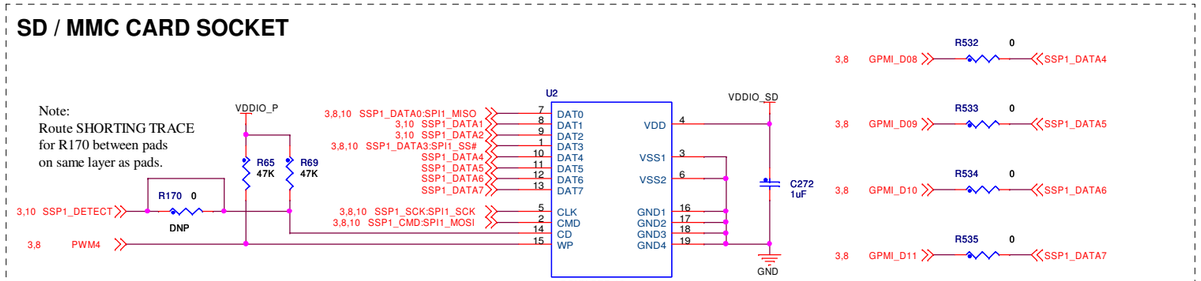
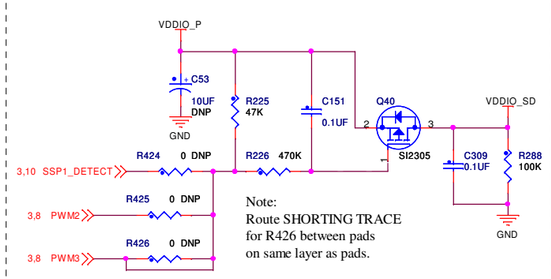
DEBUG UART SERIAL PORT



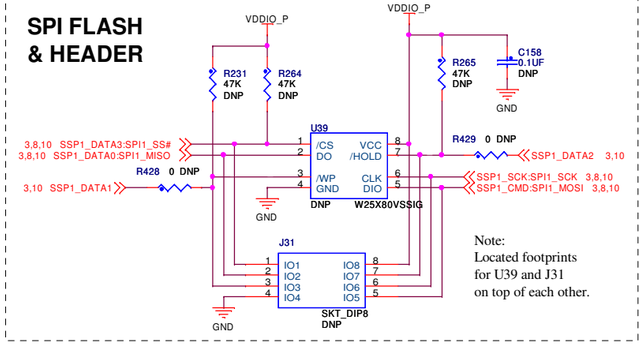
SD / MMC CARD SOCKET



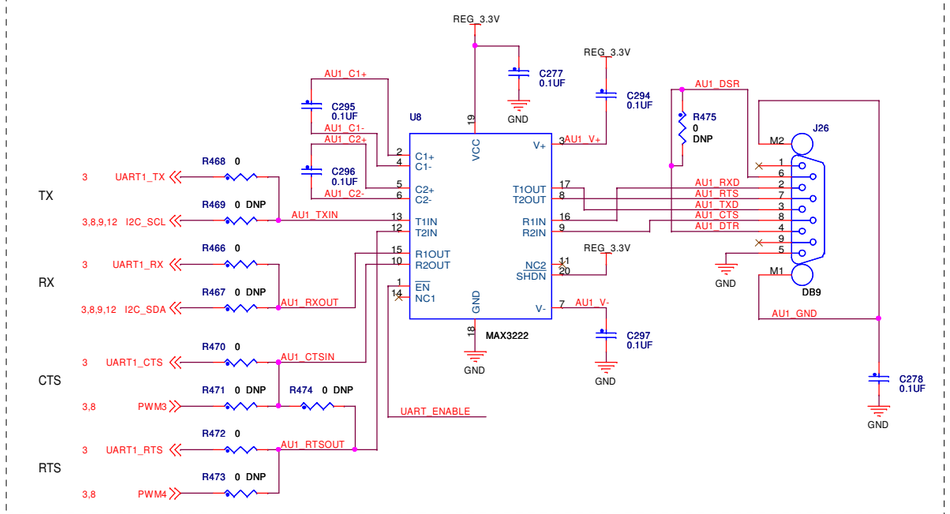
SD / MMC POWER CONTROL



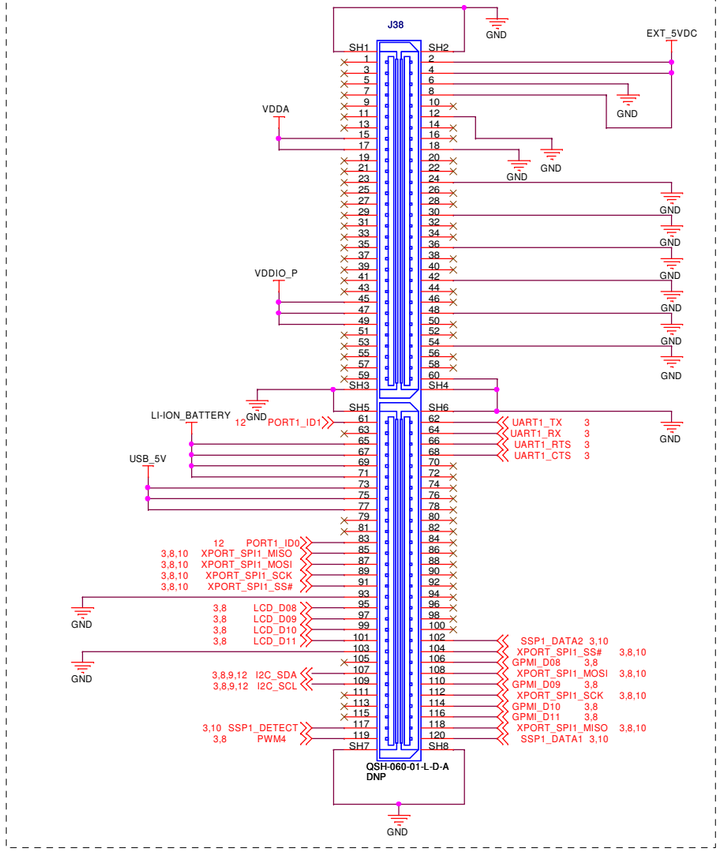
SPI FLASH & HEADER



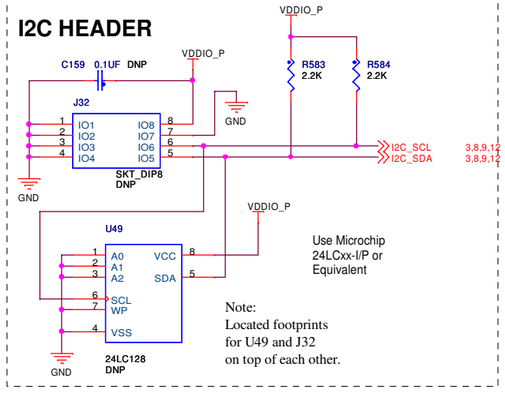
APPLICATION UART1 SERIAL PORT



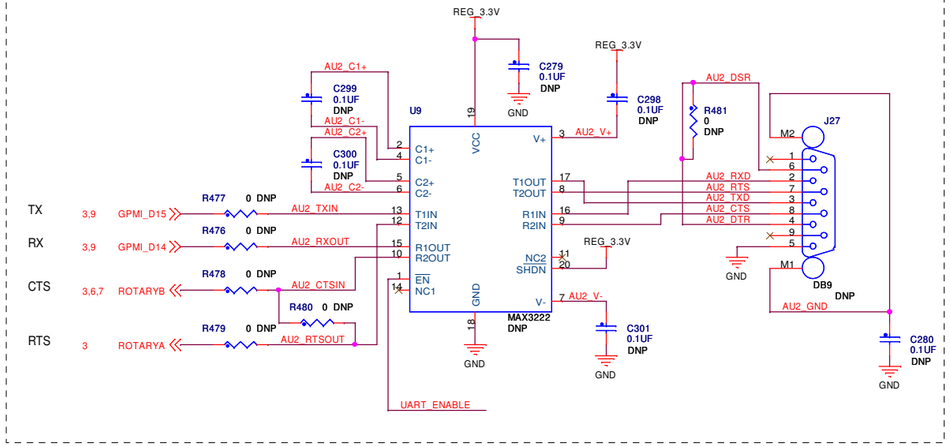
EXPANSION PORT

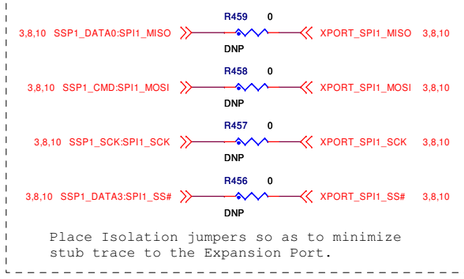


I2C HEADER



OPTIONAL APPLICATION UART2 SERIAL PORT





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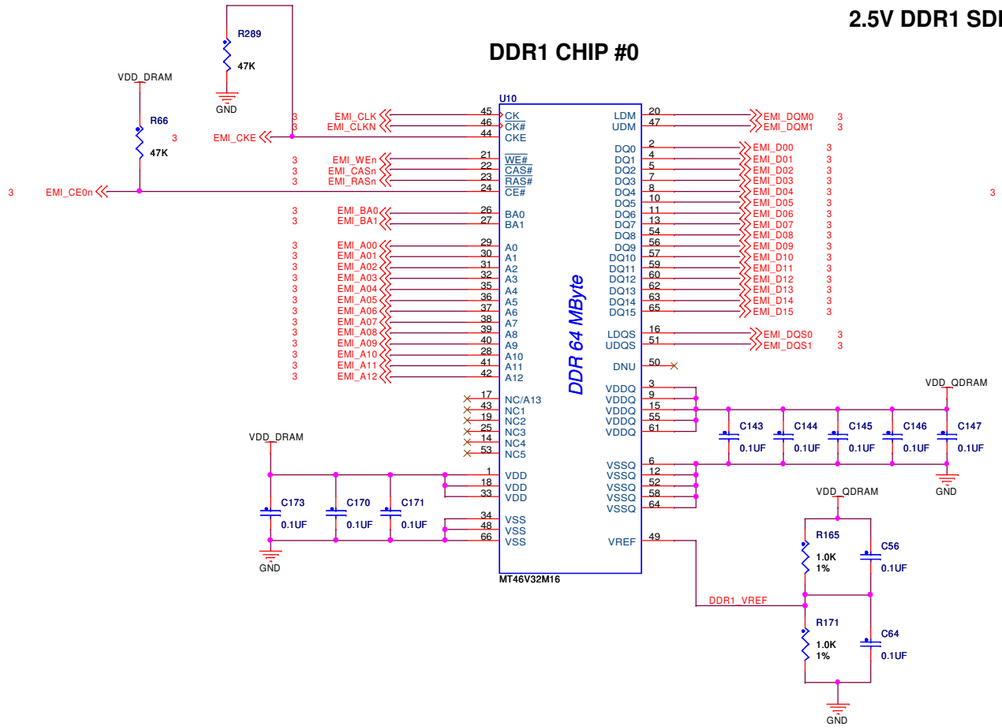
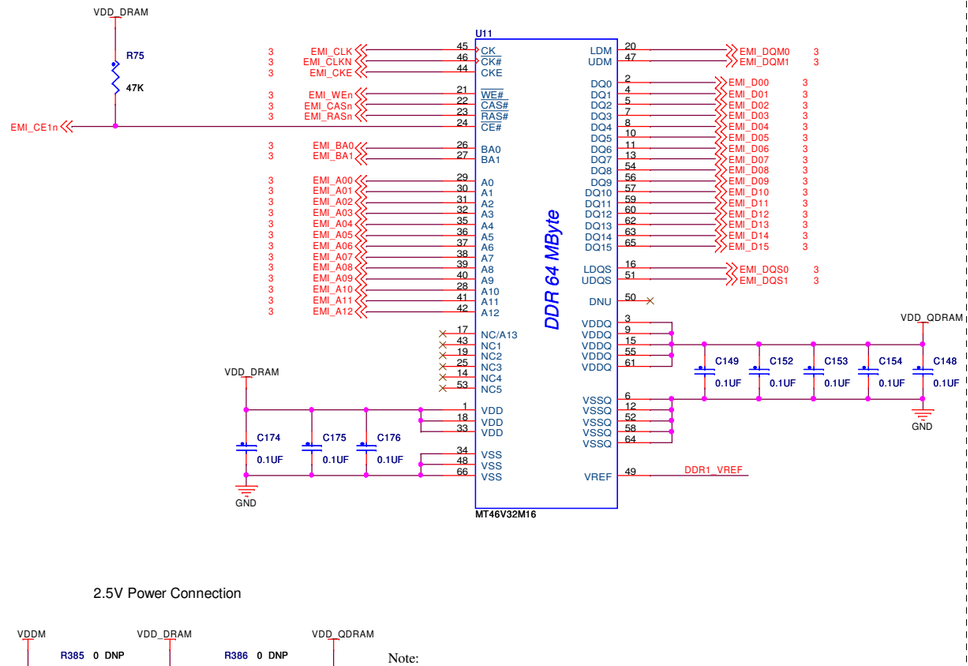
2.5V DDR1 SDRAM

DDR1 CHIP #0



DDR1 CHIP #1



2.5V Power Connection

Note:
Route SHORTING TRACE for R285 and R386 between pads on same layer as pads.

Note:
To remove power to DDR DRAM signal functions (leavind DRAM in static power state), populate Q41, R227 and R581, and cut trace across R386. This will power down signal functions when VDDIO is powered down.

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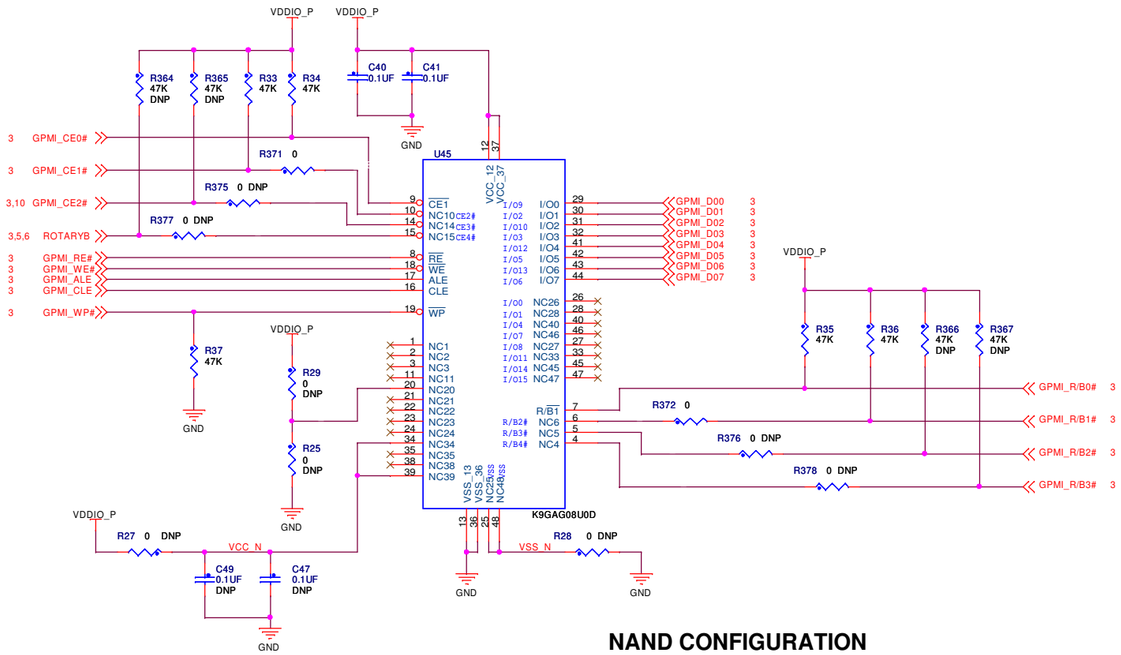
8-BIT NAND FLASH

NOTE: To support ONFI standard NAND Flash, populate R27,R28, C47, C49.
Depending on the NAND, it may also be necessary to populate either R29 or R25.



NAND CONFIGURATION

1 x Single-CE NAND	Depopulate: R33, R36, R371, R372
1 x Dual-CE NAND	Default Configuration - no change
1 x Quad-CE NAND	Populate: R33, R36, R364-R367, R371, R372, R375-R378

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **i.MX233 EVK**

Page Title: **NAND**

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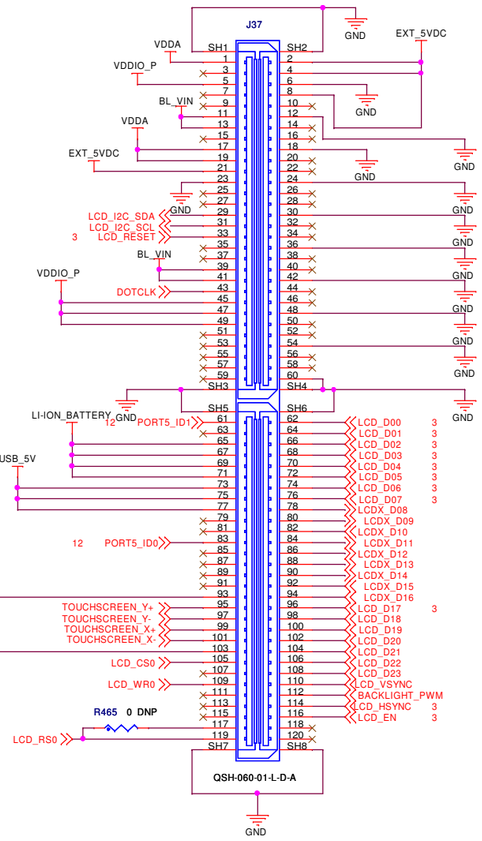
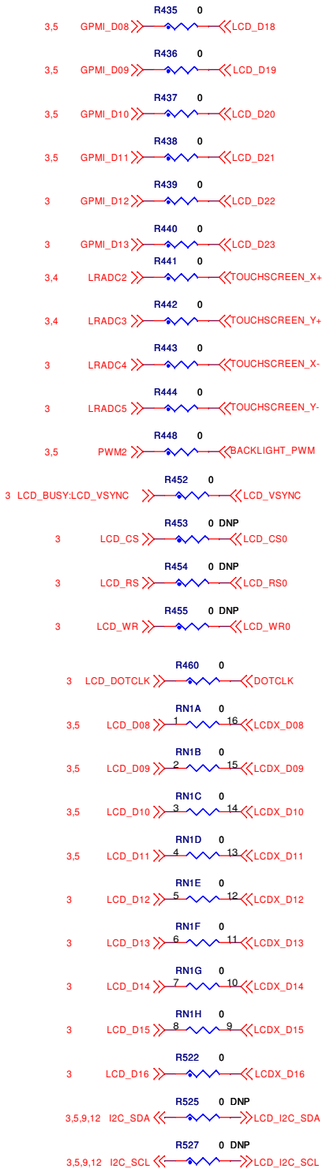
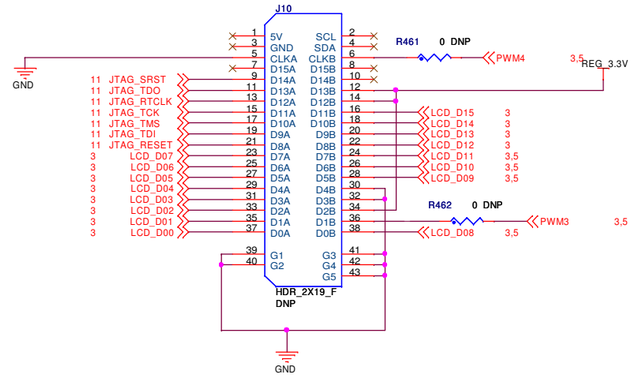
LCD Connector



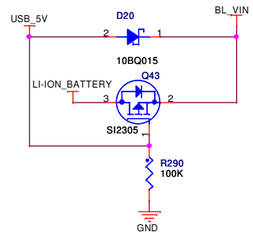
LCD Expansion Header Connections



Optional Mictor Connection Header



LCD Backlight Boost Converter Input Power Selection



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ICAP Classification: FCP: ___ FIUO: X PUBI: ___		
Drawing Title: i.MX233 EVK		
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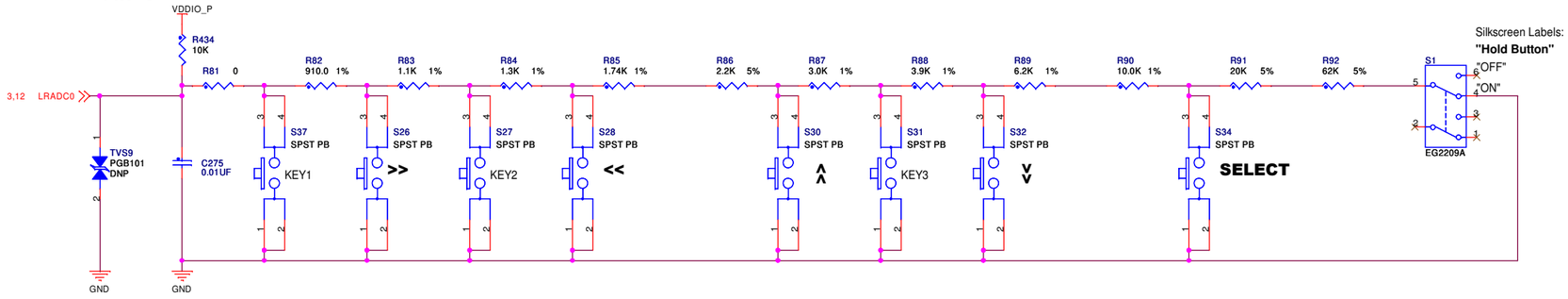
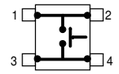
Buttons

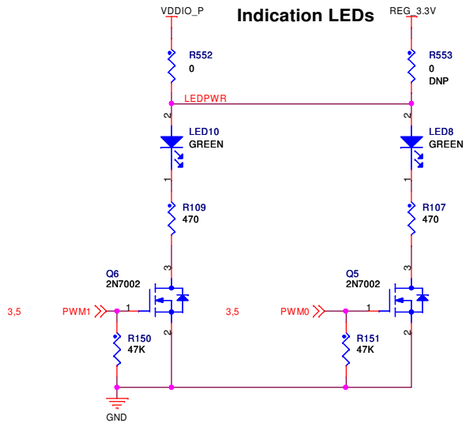


LAYOUT NOTE:

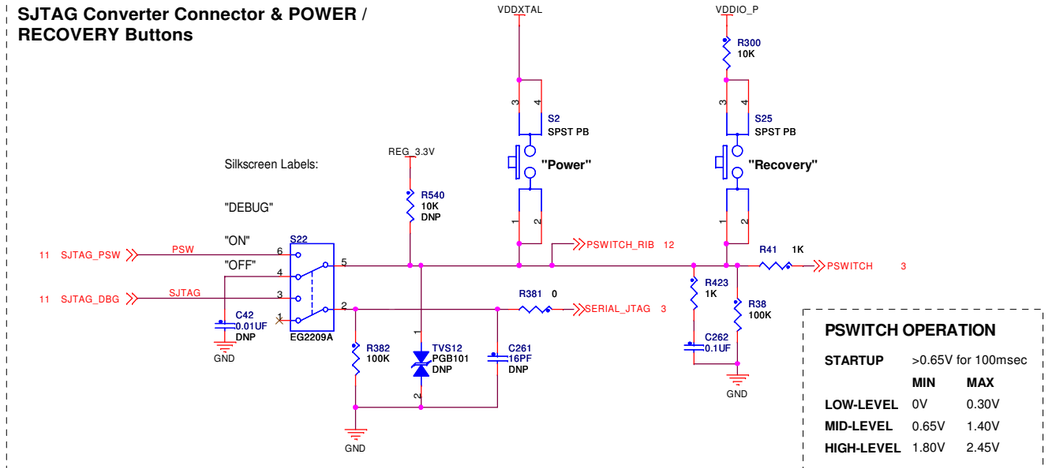


TOP VIEW
EG2526CT-ND
TACT SWITCH

Indication LEDs



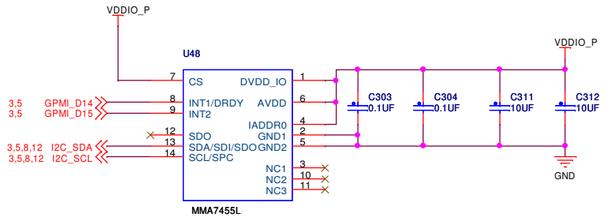
SJTAG Converter Connector & POWER / RECOVERY Buttons



PSWITCH OPERATION

STARTUP	>0.65V for 100msec	
	MIN	**MAX**
LOW-LEVEL	0V	0.30V
MID-LEVEL	0.65V	1.40V
HIGH-LEVEL	1.80V	2.45V

OPTIONAL ACCELEROMETER



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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **i.MX233 EVK**

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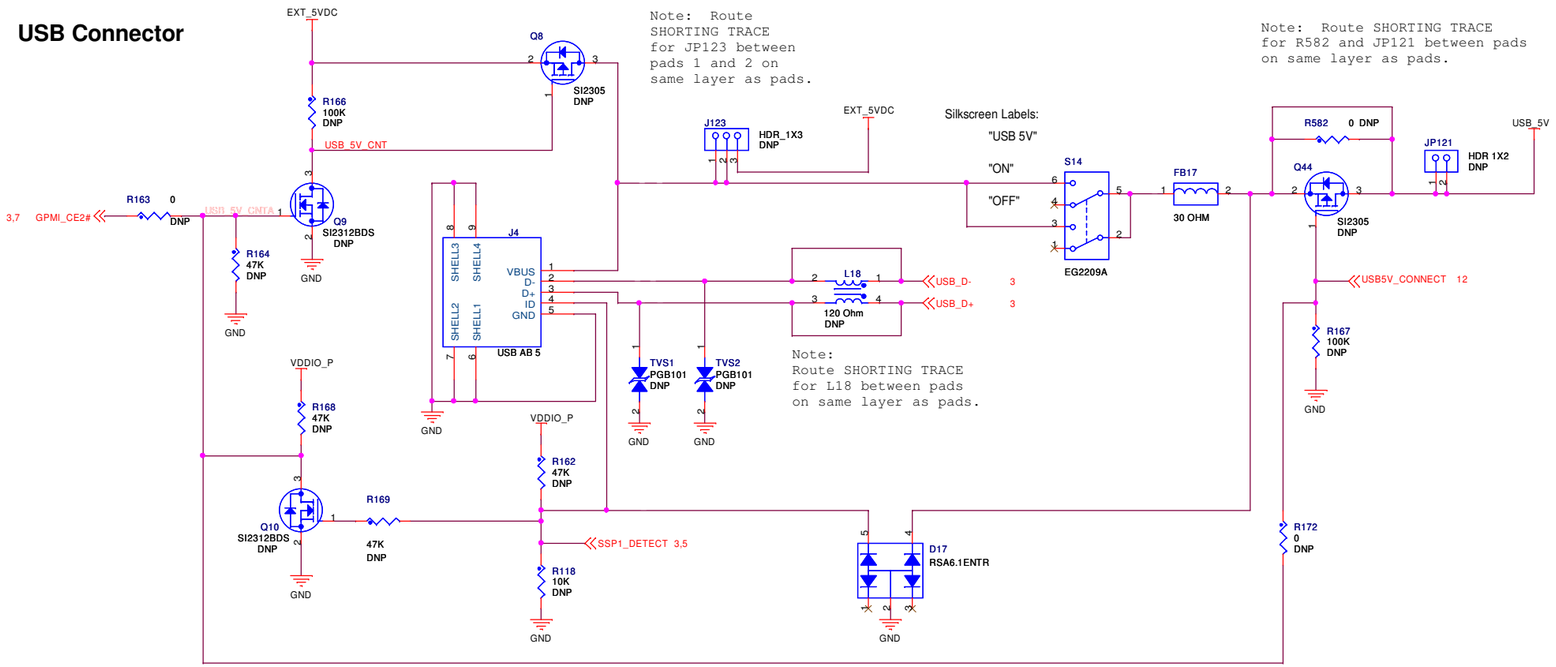
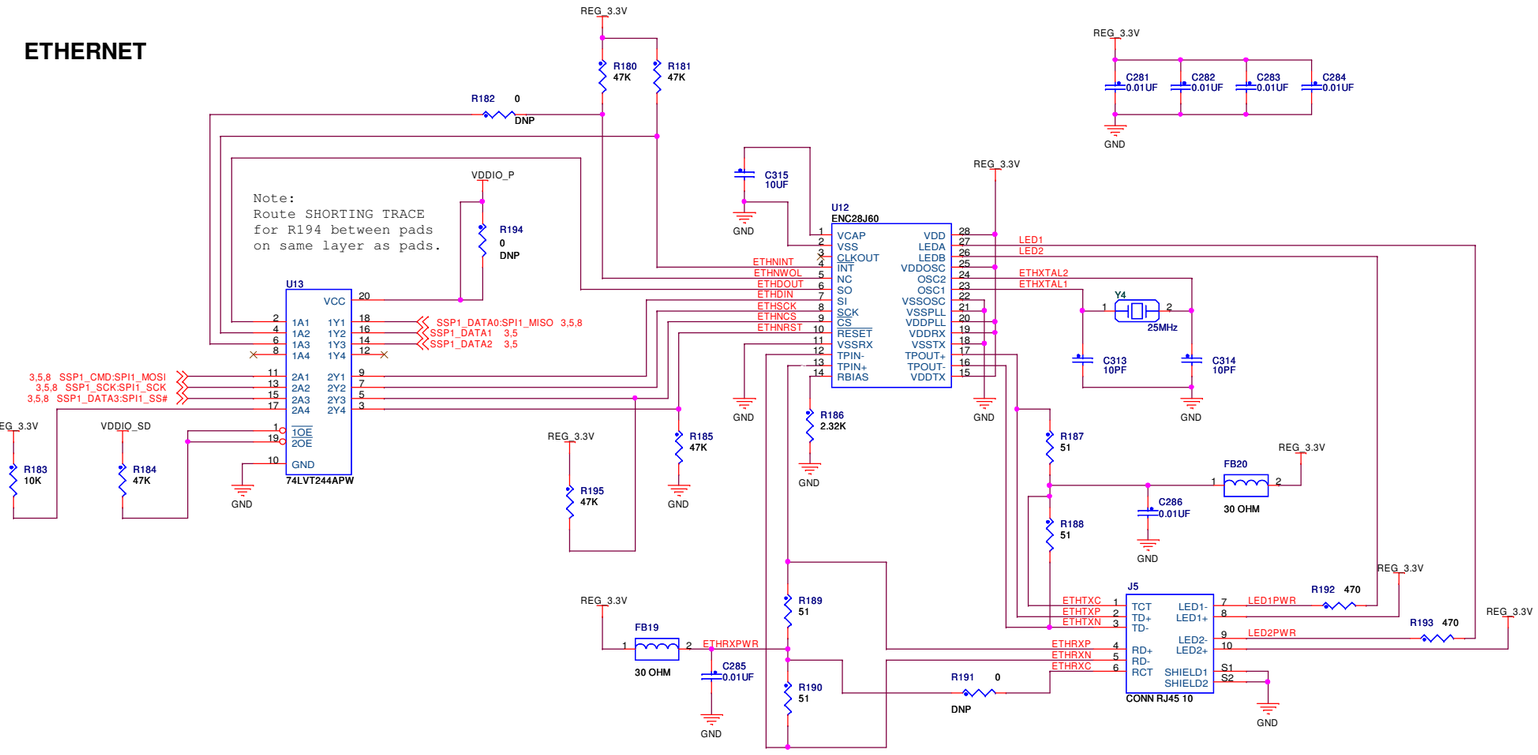
USB Connector





ICAP Classification:	FCP: ___ FIUO: X PUBI: ___
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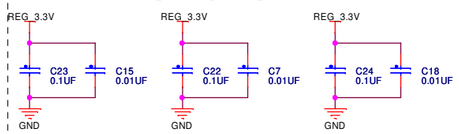
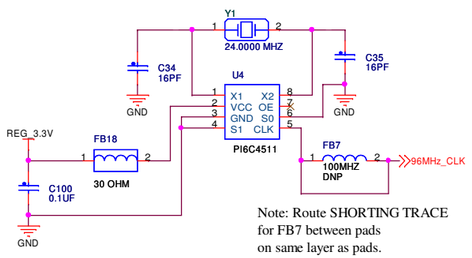
CPLD Decoupling Caps

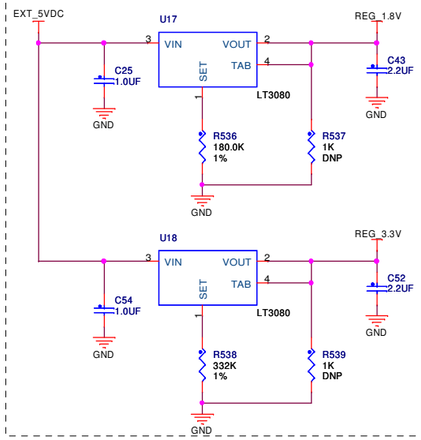


96MHz Clock Generator

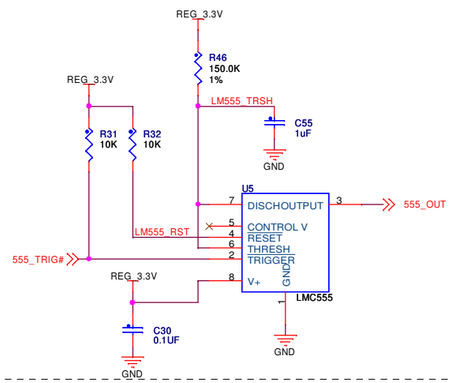


Note: Route SHORTING TRACE for FB7 between pads on same layer as pads.

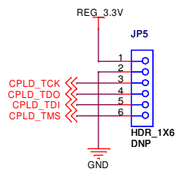
JTAG POWER



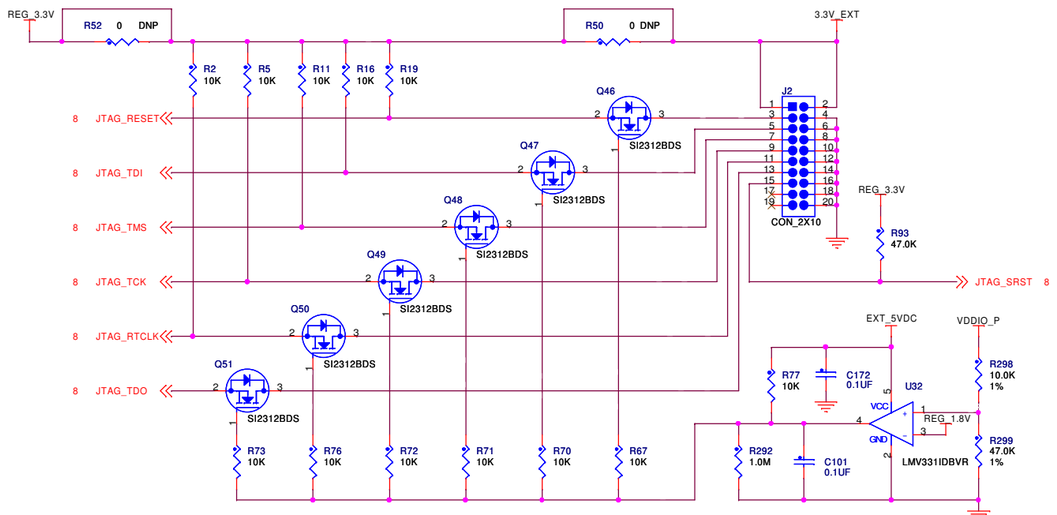
100msec Pulse Generator



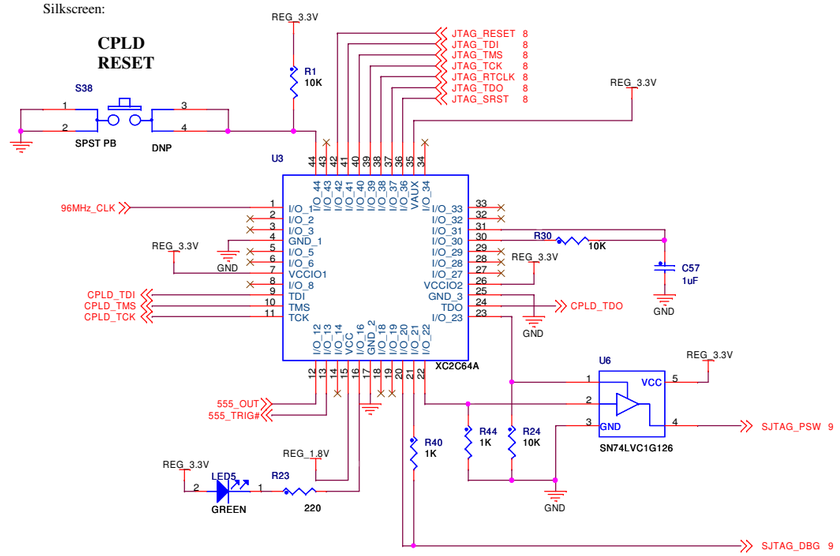
CPLD Program Header



Note: Route SHORTING TRACE for R52 and R59 between pads on same layer as pads.



Silkscreen:



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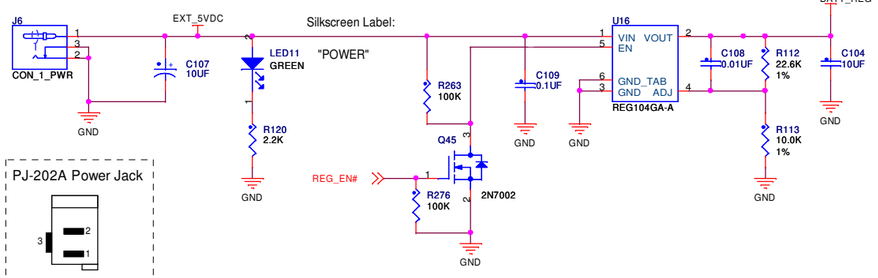
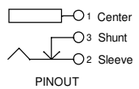
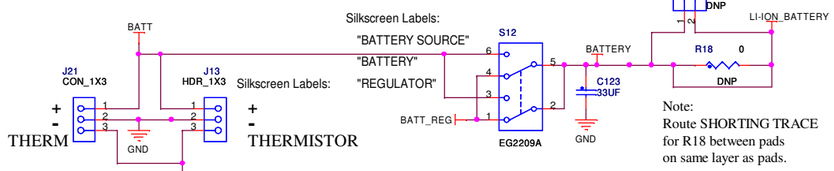
BATTERY & 5V REGULATORS



PJ-202A Power Jack

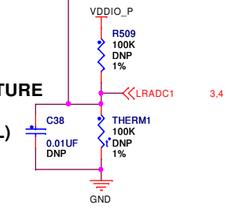


BATTERY & SOURCE SELECT SWITCH



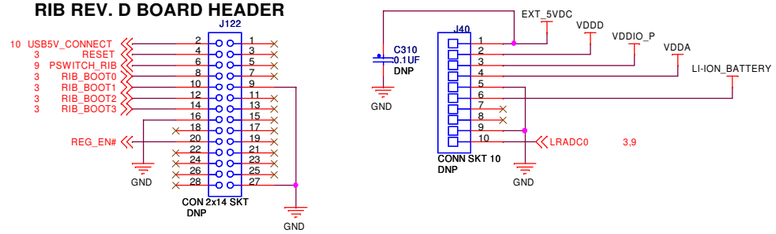
Note:
Route SHORTING TRACE
for R18 between pads
on same layer as pads.

BATTERY CHARGE TEMPERATURE SENSE (OPTIONAL)

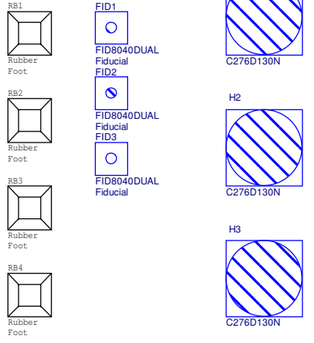


Note:
3-pin connector J21 allows the use of
aftermarket Li-ION batteries. Recommended
battery capacity is 500 - 1000 mAh.

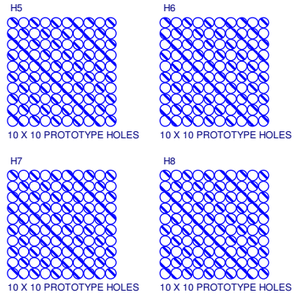
RIB REV. D BOARD HEADER



FIDUCIALS & MOUNTING HOLES



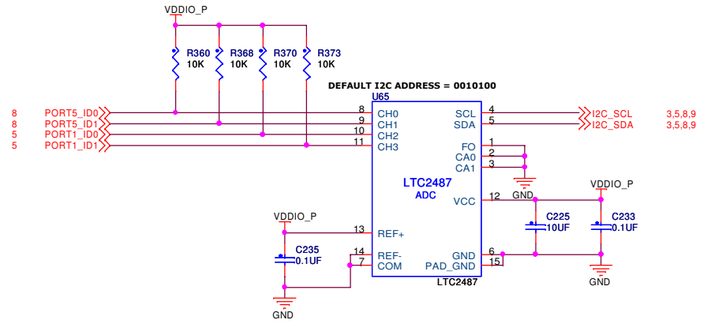
PROTOTYPING AREA 20 X 20 THROUGH HOLES



Board Mounting Holes for 4-40 screws

HARDWARE IDENTIFICATION (4-Channels)

This reduced functionality board ID circuit supports detection of one LCD port (Port 5) and one accessory port (Port 1).



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